STRUCTURE AND METHOD FOR MANUFACTURING PLANAR STRAINED SI/SIGE SUBSTRATE WITH MULTIPLE ORIENTATIONS AND DIFFERENT STRESS LEVELS

This application is related to co-assigned U.S. patent application Ser. No. 10/250,241 entitled HIGH PERFORMANCE SOI DEVICES ON HYBRID CRYSTAL-ORIENTATED SUBSTRATES, filed Jun. 17, 2003, and co-assigned U.S. patent application Ser. No. 10/710,277 (SSMP 17467, FIS920040052US1) entitled STRUCTURE AND METHOD FOR MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS, filed Jun. 30, 2004, the entire content and subject matter of which are incorporated herein by reference.

BACKGROUND OF INVENTION

The present invention relates to semiconductor materials having enhanced electron and hole mobilities, and more particularly, to semiconductor materials that include a silicon (Si)-containing layer having enhanced electron and hole mobilities. The present invention also provides methods for forming such semiconductor materials.

For more than three decades, the continued miniaturization of silicon metal oxide semiconductor field effect transistors (MOSFETs) has driven the worldwide semiconductor industry. Various showstoppers to continued scaling have been predicated for decades, but a history of innovation has sustained Moore's Law in spite of many challenges. However, there are growing signs today that metal oxide semiconductor transistors are beginning to reach their traditional scaling limits. A concise summary of near-term and long-term challenges to continued CMOS scaling can be found in the "Grand Challenges" section of the 2002 Update of the International Technology Roadmap for Semiconductors (ITRS). A very thorough review of the device, material, circuit, and systems can be found in Proc. IEEE, Vol. 89, No. 3, March 2001, a special issue dedicated to the limits of semiconductor technology.

Since it has become increasingly difficult to improve MOSFETs and therefore complementary metal oxide semiconductor (CMOS) performance through continued scaling, methods for improving performance without scaling have become critical. One approach for doing this is to increase carrier (electron and/or hole) mobilities. This can be done by either:

(1) introducing the appropriate strain into the Si lattice;

(2) by building MOSFETs on Si surfaces that are orientated in directions different than the conventional <100> Si; or

(3) a combination of (1) and (2).

As far as approach (1) is concerned, the application of stresses or strains changes the lattice dimensions of the Si-containing layer. By changing the lattice dimensions, the energy band gap of the material is changed as well. The change may only be slight in intrinsic semiconductors resulting in only a small change in resistance, but when the semiconducting material is doped, i.e., n-type, and partially ionized, a very small change in the energy bands can cause a large percentage change in the energy difference between the impurity levels and the band edge. Thus, the change in resistance of the material with stress is large.

Prior attempts to provide strain-based improvements of semiconductor substrates have utilized etch stop liners or embedded SiGe structures. N-type channel field effect transistors (nFETs) need tension on the channel for strain-based device improvements, while p-type channel field effect transistors (pFETs) need a compressive stress on the channel for strain-based device improvements.

In terms of approach (2), electrons are known to have a high mobility for a (100) Si surface orientation, but holes are known to have high mobility for a (110) surface orientation. That is, hole mobility values on (100) Si are roughly 2×–4× lower than the corresponding electron mobility for this crystallographic orientation. To compensate for this discrepancy, pFETs are typically designed with larger widths in order to balance pull-up currents against the nFET pull-down currents and achieve uniform circuit switching. NFETs having larger widths are undesirable since they take up a significant amount of chip area.

On the other hand, hole mobilities on the (110) crystal plane of Si are approximately 2× higher than on the (100) crystal plane of Si; therefore, pFETs formed on a surface having a (110) crystal plane will exhibit significantly higher drive currents than pFETs formed on a surface having a (100) crystal plane. Unfortunately, electron mobilities on the (110) crystal plane of Si are significantly degraded compared to the (100) crystal plane of Si.

There is interest in integrating strained substrates having multiple crystallographic orientations with silicon-on-insulator (SOI) technology. SOI substrates reduce parasitic capacitance within the integrated circuit, reduce individual circuit loads and reduce the incidence of latch-up, thereby improving circuit and chip performance.

In view of the state of the art mentioned above, there is a continued need for providing a strained Si/SiGe on insulator substrate with multiple crystallographic orientations and different stress levels.

SUMMARY OF THE INVENTION

One object of the present invention is to provide a multiple crystallographic orientation strained Si/SiGe-on-insulator (SGOI) substrate.

Another object of the present invention is to provide a SGOI substrate that integrates strained silicon nFETs on a (100) crystal plane with strained silicon pFETs on a (110) crystal plane.

These and other objects and advantages are achieved in the present invention by utilizing a method that provides a multiple orientation strained SGOI substrate including bonding, masking, etching and epitaxial regrowth process steps. Specifically, the method of the present invention comprises the steps of:

providing an initial structure having a first device region and a second device region positioned on and separated by an insulating material, said first device region comprising a first orientation material and said second device region comprising an insulating layer atop a second orientation material, wherein said first orientation material and said second orientation material have different crystallographic orientations;

forming a first concentration of lattice modifying material atop said first orientation material;

forming a protective layer atop said first concentration of lattice modifying material;

removing said insulating layer atop said second orientation material; forming a second concentration of said lattice modifying material atop said second orientation material;

removing said protective layer from said first concentration of lattice modifying material;